80C51 FAMILY INSTRUCTION SET

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Philips Semiconductors

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80C51 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings[1]

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ORL C,bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

[1]Note that operations on SFR byte address 208 or bit addresses 209–215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

Rn	Register R7–R0 of the currently selected Register Bank.
direct	8–bit internal data location's address. This could be an Internal Data RAM location (0–127) or a SFR [i.e., I/O port, control register, status register, etc. (128–255)].
@Ri	8–bit internal data RAM location (0–255) addressed indirectly through register R1 or R0.
#data	8–bit constant included in the instruction.
#data 16	16–bit constant included in the instruction
addr 16	16–bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k–byte Program Memory address space.
addr 11	11–bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k–byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8–bit offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.
bit	Direct Addressed bit in Internal Data RAM or Special Function Register.

MNEMONIC		DESCRIPTION	BYTE	MACHINE CYCLES
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with carry	1	1
ADDC	A,direct	Add direct byte to Accumulator with carry	2	1
ADDC	A,@Ri	Add indirect RAM to Accumulator with carry	1	1
ADDC	A,#data	Add immediate data to A_{CC} with carry	2	1
SUBB	A,Rn	Subtract Register from A_{CC} with borrow	1	1
SUBB	A,direct	Subtract direct byte from A_{CC} with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A_{CC} with borrow	1	1
SUBB	A,#data	Subtract immediate data from A_{CC} with borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1

80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	MACHINE CYCLES
ARITHMETIC OPERATIONS (Continued)				
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement Register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1
LOGICAL OPERATIONS				
ANL	A,Rn	AND Register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive–OR register to Accumulator	1	1
XRL	A,direct	Exclusive–OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive–OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive–OR immediate data to Accumulator	2	1
XRL	direct,A	Exclusive–OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive–OR immediate data to direct byte	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator left	1	1
RLC	A	Rotate Accumulator left through the carry	1	1
RR	A	Rotate Accumulator right	1	1
RRC	A	Rotate Accumulator right through the carry	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1

80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	MACHINE CYCLES
DATA TRANSFER (Continued)				
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	RN,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16–bit constant	3	2
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A_{CC}	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A_{CC}	1	2
MOVX	A,@Ri	Move external RAM (8–bit addr) to A_{CC}	1	2
MOVX	A,@DPTR	Move external RAM (16–bit addr) to A_{CC}	1	2
MOVX	@Ri,A	Move A_{CC} to external RAM (8–bit addr)	1	2
MOVX	@DPTR,A	Move A_{CC} to external RAM (16–bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange low–order digit indirect RAM with A_{CC}	1	1
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear carry	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry	2	1
MOV	bit,C	Move carry to direct bit	2	2
JC	rel	Jump if carry is set	2	2
JNC	rel	Jump if carry not set	2	2

80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	MACHINE CYCLES
BOOLEAN VARIABLE MANIPULATION (Continued)				
JB	rel	Jump if direct bit is set	3	2
JNB	rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
PROGRAM BRANCHING				
ACALL	addr11	Absolute subroutine call	2	2
LCALL	addr16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute jump	2	2
LJMP	addr16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is zero	2	2
JNZ	rel	Jump if Accumulator is not zero	2	2
CJNE	A,direct,rel	Compare direct byte to A_{CC} and jump if not equal	3	2
CJNE	A,#data,rel	Compare immediate to A_{CC} and jump if not equal	3	2
CJNE	RN,#data,rel	Compare immediate to register and jump if not equal	3	2
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	2
NOP		No operation	1	1

Please note:

- In a Philips 80C51 device running in **12-clock mode**, **1 machine cycle = 12 oscillator clock cycles**.
- In a Philips 80C51 device running in **6-clock mode**, **1 machine cycle = 6 oscillator clock cycles**.
- In a Philips **LPC900** family device, **1 machine cycle = 2 oscillator clock cycles**.