# 80C51 FAMILY INSTRUCTION SET

2002 Oct 16



Philips Semiconductors

# 80C51 FAMILY INSTRUCTION SET

#### 80C51 Instruction Set Summary

		interrupt ree	sponoo	rime.		to Hardware Descri	p	ipici.		
		l	Instruc	tions	that Af	ffect Flag Settings	(1)			
		Instruction		Flag	9	Instruction		Flag		
			С	٥v	AC		С	ov	AC	
		ADD	Х	Х	Х	CLR C	0			
		ADDC SUBB		X X	X X	CPL C ANL C,bit	X X			
		MUL	0	x	~	ANL C,/bit	x			
		DIV	0	Х		ORL C,bit	Х			
		DA	X			ORL C,/bit	Х			
		RRC RLC	X X			MOV C,bit CJNE	X X			
		SETB C	1			00.12				
Note that ope	rations on SFR byte a	ddress 208 or bit add	resses	209–2 <sup>-</sup>	15 (i.e.	, the PSW or bits in	the PSV	V) will	also affect fl	ag settings.
		Notes	s on ins	structi	ion set	t and addressing r	nodes:			
Rn	Register R7–R	R0 of the currently sele	ected R	egister	r Bank.					
direct		data location's addres s register, etc. (128–2		could I	be an I	nternal Data RAM	ocation (	0–127	) or a SFR [i	.e., I/O port, control
@Ri	8-bit internal of	data RAM location (0-	-255) ad	dress	ed indi	rectly through regis	ter R1 or	R0.		
#data	8-bit constant	included in the instrue	ction.							
#data 16 16-bit constant included in the instruction										
addr 16	16-bit destina	tion address. Used by		and I			www.horov	vithin	the Call hute	Dragram Mamani
addi i o	address space				JIMP.	A branch can be ar	lywnere v	within	INE 64K-Dyte	Program Memory
addr 11	address space 11-bit destina	).	/ ACALI				-			age of program memory
	address space 11–bit destina as the first byt Signed (two's	e. tion address. Used by e of the following instr	ACALI ruction.	_ and A	AJMP.	The branch will be	within th	e sam	e 2k–byte pa	
addr 11	address space 11–bit destina as the first byt Signed (two's first byte of the	e. tion address. Used by e of the following instr complement) 8–bit off	ACALI ruction.	_ and <i>I</i>	AJMP. d by S.	The branch will be	within th	e sam	e 2k–byte pa	age of program memory
addr 11 rel	address space 11–bit destina as the first byt Signed (two's first byte of the	<ul> <li>a.</li> <li>address. Used by</li> <li>e of the following instr</li> <li>complement) 8-bit off</li> <li>a following instruction.</li> </ul>	ACALI ruction.	- and A e. Used or Spec	AJMP. d by S.	The branch will be JMP and all conditi nction Register.	within th	e sam os. Ra	e 2k–byte pa	age of program memory
addr 11 rel bit	address space 11–bit destina as the first byt Signed (two's first byte of the Direct Address	<ul> <li>a.</li> <li>address. Used by</li> <li>e of the following instr</li> <li>complement) 8-bit off</li> <li>a following instruction.</li> </ul>	ACALI ruction.	- and A e. Used or Spec	AJMP. d by S. cial Fu	The branch will be JMP and all conditi nction Register.	within th	e sam os. Ra	e 2k–byte pa nge is -128 t	age of program memory o +127 bytes relative to
addr 11 rel bit	address space 11-bit destina as the first byt Signed (two's first byte of the Direct Address MNEMONIC	<ul> <li>a.</li> <li>address. Used by</li> <li>e of the following instr</li> <li>complement) 8-bit off</li> <li>a following instruction.</li> </ul>	v ACALI ruction. fset byte	and A e. Used or Spec DES	AJMP. d by S. cial Fu SCRIPT	The branch will be JMP and all conditi nction Register.	within th	e sam os. Ra	e 2k–byte pa nge is -128 t	age of program memory o +127 bytes relative to
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addr 11 rel bit RITHMETIC ( ADD ADD ADD	address space 11-bit destina as the first byt Signed (two's first byte of the Direct Address MNEMONIC OPERATIONS A,Rn A,direct A,@Ri	a. tion address. Used by e of the following instr complement) 8-bit off e following instruction. sed bit in Internal Data Add registe Add direct I Add indirect	r ACALI ruction. a RAM of a RAM of er to Acc byte to Acc byte to Acc byte to Acc	and A	AJMP. d by S. cial Fui SCRIP1 ator nulator umulator ccumu	The branch will be JMP and all conditi nction Register. TION	within th	e sam os. Ra	e 2k-byte pa nge is -128 t BYTE 1 2 1	age of program memory o +127 bytes relative to MACHINE CYCLES 1 1 1
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## 80C51 Instruction Set Summary (Continued)

	MNEMONIC	DESCRIPTION	BYTE	MACHINE CYCLES
ARITHMET	IC OPERATIONS (Continu	Jed)		
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	А	Decrement Accumulator	1	1
DEC	Rn	Decrement Register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	А	Decimal Adjust Accumulator	1	1
	PERATIONS			
ANL	A,Rn	AND Register to Accumulator	1	1
			2	
ANL	A,direct	AND direct byte to Accumulator		1
ANL	A,@Ri	AND indirect RAM to Accumulator	1 2	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	3	•
ANL	direct,#data	AND immediate data to direct byte		2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive–OR register to Accumulator	1	1
XRL	A,direct	Exclusive–OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive–OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive–OR immediate data to Accumulator	2	1
XRL	direct,A	Exclusive–OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive–OR immediate data to direct byte	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator left	1	1
RLC	A	Rotate Accumulator left through the carry	1	1
RR	A	Rotate Accumulator right	1	1
RRC	A	Rotate Accumulator right through the carry	1	1
SWAP	Α	Swap nibbles within the Accumulator	1	1
DATA TRAI	NSFER			
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1

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#### 80C51 Instruction Set Summary (Continued)

	MNEMONIC	DESCRIPTION	BYTE	MACHINE CYCLES
DATA TRAI	NSFER (Continued)			
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	RN,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct, direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to Acc	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to Acc	1	2
MOVX	A,@Ri	Move external RAM (8–bit addr) to $A_{cc}$	1	2
MOVX	A,@DPTR	Move external RAM (16–bit addr) to $A_{cc}$	1	2
MOVX	@Ri,A	Move A <sub>cc</sub> to external RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A <sub>cc</sub> to external RAM (16–bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
ХСН	A,Rn	Exchange register with Accumulator	1	1
ХСН	A,direct	Exchange direct byte with Accumulator	2	1
ХСН	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with $A_{\mbox{\tiny CC}}$	1	1
BOOLEAN	VARIABLE MANIPULATIO	N		
CLR	С	Clear carry	1	1
CLR	bit	Clear direct bit	2	1
SETB	С	Set carry	1	1
SETB	bit	Set direct bit	2	1
CPL	С	Complement carry	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry	2	1
MOV	bit,C	Move carry to direct bit	2	2
JC	rel	Jump if carry is set	2	2
JNC	rel	Jump if carry not set	2	2

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80C51 Instruction Set S	ummary (Continued)
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	MNEMONIC	DESCRIPTION	BYTE	MACHINE CYCLES		
BOOLEAN VARIABLE MANIPULATION (Continued)						
JB	rel	Jump if direct bit is set	3	2		
JNB	rel	Jump if direct bit is not set	3	2		
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2		
PROGRAM	BRANCHING					
ACALL	addr11	Absolute subroutine call	2	2		
LCALL	addr16	Long subroutine call	3	2		
RET		Return from subroutine	1	2		
RETI		Return from interrupt	1	2		
AJMP	addr11	Absolute jump	2	2		
LJMP	addr16	Long jump	3	2		
SJMP	rel	Short jump (relative addr)	2	2		
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2		
JZ	rel	Jump if Accumulator is zero	2	2		
JNZ	rel	Jump if Accumulator is not zero	2	2		
CJNE	A,direct,rel	Compare direct byte to $A_{cc}$ and jump if not equal	3	2		
CJNE	A,#data,rel	Compare immediate to $A_{\mbox{\tiny CC}}$ and jump if not equal	3	2		
CJNE	RN,#data,rel	Compare immediate to register and jump if not equal	3	2		
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2		
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2		
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	2		
NOP		No operation	1	1		

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### Please note:

- In a Philips 80C51 device running in 12-clock mode, 1 machine cycle = 12 oscillator clock cycles.
- In a Philips 80C51 device running in 6-clock mode, 1 machine cycle = 6 oscillator clock cycles.
- In a Philips LPC900 family device, 1 machine cycle = 2 oscillator clock cycles.