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Selected papers from the 10th International Conference on Application of Concurrency to System Design (ACSD 2010)

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Editorial

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The articles in this Special Issue of IET Computers & Digital Techniques are revised and extended versions of selected papers presented at the 10th International Conference on Application of Concurrency to System Design (ACSD'10) held in Braga, Portugal, on 21–25 June 2010. The ACSD conference series serves a forum for disseminating theoretical results, advanced methods and tools for the design of complex concurrent systems. The main aim of the conference is to bring theory and practice closer together by informing practitioners of the latest theoretical results, and challenging theoreticians with complex industrial problems. It therefore welcomes both academic and industrial participants.

The five articles in this Special Issue have been selected from the 22 papers accepted for presentation at ACSD'10, based on the reviews by the Programme Committee. These papers have been extended and underwent two further rounds of reviewing.

In this Special Issue, the contributions have been divided into two groups. The first group comprises three articles and is concerned with synthesis of VLSI circuits. The second group comprises two papers and is concerned with formal verification of concurrent systems.

The first paper, by Andrey Mokhov, Arseniy Alekseyev, and Alex Yakovlev, presents a formal method and a software tool for encoding instruction sets of processors, facilitating the design of efficient decoders, targeting various design optimality criteria. The method is based on the Conditional Partial Order Graph (CPOG) formalism developed by the authors. The ACSD'10 version of this paper received the best paper award.

The second paper, by Dominic Wist, Mark Schaefer, Walter Vogler, and Ralf Wollowski, presents a method for logic synthesis of large asynchronous circuits. This method tackles the associated state space explosion by decomposing the original specification. In order to mitigate the problem of encoding conflicts arising because of decomposition, internal communication between the components is introduced.

The third paper, by Wei Song, Doug Edwards, Zhenyu Liu, and Sohini Dasgupta, presents a novel asynchronous dispatching algorithm for general three-stage Clos networks. It outperforms the synchronous concurrent round-robin dispatching algorithm. It is also better in terms of area and power consumption than its synchronous version.

The fourth paper, by Matthias Raffelsieper, MohammadReza Mousavi, and Hans Zantema, presents a set of criteria on vector-based transition systems, which guarantee the next state computation to be independent on the execution order of microsteps. If these criteria are satisfied, the state-space exploration algorithm only needs to consider one representative among all possible permutations of micro-steps, which can greatly increase its efficiency. The authors also customise their technique so that it can ignore the start-up phase and focus on the long-run behaviour.

The fifth paper, by Tuomas Launiainen, Keijo Heljanko, and Tommi Junttila, presents an efficient approach to verify safety properties expressed in PSL (IEEE Std 1850 Property Specification Language), which can also be used as a sound, but incomplete, bug hunting tool for general (non-safety) PSL properties. The presented approach handles a larger syntactic subset of PSL safety properties than other existing methods.

We appreciate the work of the authors and are grateful to the reviewers for their constructive criticism that helped to improve the articles presented in this Special Issue.

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Guest Co-Editors

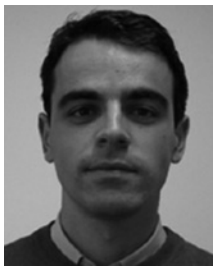
Luís Gomes received his Electrotech. Eng. degree from Universidade Técnica de Lisboa, Lisbon, Portugal, in 1981, and a PhD degree in Digital Systems from Universidade Nova de Lisboa, in 1997. He is currently Associate Professor at the Electrical Engineering Department, Faculty of Sciences and Technology of

Universidade Nova de Lisboa, Portugal and a researcher at UNINOVA Institute, Portugal. From 1984 to 1987, he was with the R&D engineering department of EID, a Portuguese medium sized enterprise, working in the area of electronic system design. He was made a 'Profesor Onorific', at Transilvanea University of Brasov, Romania in 2007.

His main interests include the usage of Petri nets and other concurrency models, applied to reconfigurable and embedded systems co-design.

He was co-editor of the books 'Hardware Design and Petri Nets' (Kluwer Academic Publishers, 2000), 'Advances on remote laboratories and e-learning experiences' (University of Deusto, 2007), and 'Behavioral Modeling for Embedded Systems and Technologies: Applications for Design and Implementation' (IGI Global, 2009).

Victor Khomenko obtained his MSc with distinction in Computer Science, Applied Mathematics and Teaching of Mathematics and Computer Science in 1998 from Kiev Taras Shevchenko University, and PhD in Computing Science in 2003 from Newcastle University. He was a Program Committee Chair for the International Conference on Application of Concurrency to System Design (ACSD'10). He also organised the Workshop on UnFOlding and partial order techniques (UFO'07) and Workshop on BALSA Re-Synthesis (RESYN'09). In January 2005 Victor became a Lecturer in the School of Computing Science, Newcastle University, and in September 2005 he obtained a Royal Academy of Engineering / EPSRC Post-doctoral Research Fellowship and worked on the Design and Verification of Asynchronous Circuits (DAVAC) project. After the end of this award, in September 2010, he switched back to Lectureship. Victor's research interests include model checking of Petri nets, Petri net unfolding techniques, verification and synthesis of self-timed (asynchronous) circuits.



João M. Fernandes is an Associate Professor (with Habilitation) at the Dept. Informatics, Universidade do Minho. He conducts his research activities in Software Engineering, with a special interest in Software Modeling, Requirements Engineering, and Embedded Software. In May 2000, he finished his Ph.D. dissertation, where he proposed a UML-based approach to develop embedded systems. During his Ph.D. and now as part of his research and teaching activities, his work is focused on the methodological and technologic aspects related with the use of a multi-perspective, model-driven approach for developing embedded systems. From Sep/2002 until Feb/2003, he was a post-doctoral researcher at the Embedded Systems Laboratory, TUCS, in Turku, Finland, and from Sep/2006 until Jun/2007, he was an invited assistant professor at Dept. Computer Science, Aarhus University, Denmark. He is the author of more than 90 papers published in journals, books and conference proceedings and co-editor of the book 'Behavioral Modeling for Embedded Systems and Technologies: Applications for Design and Implementation' (IGI Global, 2009). Dr. Fernandes is member of the Editorial Review Board of the Journal of Information Technology Research, IGI Publishing, since Jun/2007. He has been involved in the organisation of various international events, including the 3rd Int. Conf. on Application of Concurrency to System Design (ACSD 2003), the 5th IFIP Int. Conf. on Distributed and Parallel Embedded Systems (DIPES 2006), the 3rd Int. Summer School on Generative and Transformational Techniques in Software Engineering (GTTSE 2009), and the Model-based Methodologies for Pervasive and Embedded Software (MOMPES) workshops series.

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